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10/675,960	10/02/2003	Hirokazu Sekine	243472US2TTC	5929

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EXAMINER	
GEBRIEL, SELAM T	

ART UNIT	PAPER NUMBER
2622	

NOTIFICATION DATE	DELIVERY MODE
03/21/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/675,960	SEKINE, HIROKAZU	
	Examiner	Art Unit	
	SELAM T. GEBRIEL	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *12/11/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1 – 23 are rejected under 35 U.S.C. 102(e) as being anticipated by Hashimoto (US 6,956,605 B1).

3. Regarding claim 1, Hashimoto discloses a CMOS image sensor (Figure 1) according to an embodiment of the present invention comprises:

A plurality of unit cells (Figure 21, Element 81) arranged in the row and column directions at a predetermined pitch respectively in a two-dimensional plain forming a matrix (Col 13, Line 62 – 67) which include:

A first and a second photoelectric conversion element (Figure 1, Element a11 and Element a22),

A first and a second transfer transistor (Figure 1, Element MTX3 and Element MTX2) for transferring charges stored by the photoelectric conversion elements at their common floating junctions (Col 13, Line 59 – 67 to Col 14, Line 1 – 65);

Reset transistors (Figure 1, Element MRES) for resetting the potential of the floating junctions

Driver transistors (Figure 1, Element MSF) whose output potential is controlled by the potential of the floating junctions, and

Address transistors (Figure 1, Element MSEL) for selectively driving the driver transistors;

Reset drain voltage lines (Figure 22, Element 112) provided in the column direction of the matrix arrangement for resetting the potential of the common floating junctions included in the unit cell belonging to each column of the matrix arrangement (Col 13, Line 59 – 67 to Col 14, Line 1 – 65);

First transfer lines (Figure 22, Element 108a) provided in the row direction of the matrix arrangement for controlling the first transfer transistor included in the unit cell belonging to each row (See Figure 2, 21 – 22, Col 13, Line 59 – 67 to Col 14, Line 1 – 65);

Second transfer lines (Figure 22, Element 108c) in the row direction of the matrix arrangement for controlling the second transfer transistors included in the unit cells belonging to each row of the matrix arrangement (See Figure 2, 21 – 22 , Col 13, Line 59 – 67 to Col 14, Line 1 – 65);

Signal output lines (Figure 22, Element 107) provided in the column direction of the matrix arrangement to which the output voltages of the driver transistors included in the unit cells belonging to each column of the matrix arrangement are supplied (See Figure 2, 21 – 22, Col 13, Line 59 – 67 to Col 14, Line 1 – 65), and

Address lines (Figure 22, Element 110) provided in the row direction of the matrix arrangement for selectively driving the drives transistors included in the unit cell belonging to each row (See Figure 2, 21 – 22 , Col 13, Line 59 – 67 to Col 14, Line 1 – 65).

4. Regarding claim 2, A CMOS image sensor according to Claim 1, wherein:

A first pixel line (Col 8, Line 60 – 67 to Col 9 Line 1 – 8) composed of the first photoelectric conversion element included in the unit cells belonging to each row of the matrix arrangement (See Figure 2, 21 – 22 and Col 13, Line 59 – 67 to Col 14, Line 1 – 65) and

A second pixel lines (Col 8, Line 60 – 67 to Col 9 Line 1 – 8) composed of the second photoelectric conversion element included in the unit cells are independently read respectively by the first and second transfer lines (See Figure 2, 21 – 22 and Col 13, Line 59 – 67 to Col 14, Line 1 – 65).

5. Regarding claim 3, A CMOS image sensor according to Claim 2, wherein:

The first pixel lines and the second pixel lines (Col 8, Line 60 – 67 to Col 9 Line 1 – 8) are read by switching the first and second transfer transistors by the first and second transfer lines (See Figure 2, 21 – 22 and Col 13, Line 59 – 67 to Col 14, Line 1 – 65).

6. Regarding claim 4, A CMOS image sensor according to Claim 3, wherein:

The driver transistors (Figure 1, Element MSF) and the address transistors (Figure 1, Element MSEL) which are included in the respective unit cells are connected in series, wherein the first and second photoelectric conversion elements are connected to gate electrodes of the driver transistors via the first and second transfer transistors, and wherein source electrodes of the reset transistors are connected to the gate electrodes of the driver transistors (See Figure 2, Col 3 Line 43 - 63 and see Figure 21 and 22, Col 13, Line 59 – 67 to Col 14, Line 1 – 65).

7. Regarding claim 5, A CMOS image sensor according to Claim 4, wherein the first and second photoelectric conversion elements are photodiodes (Figure 21, Element 82a – 82d are photodiodes).

8. Regarding claim 6, A CMOS image sensor according to Claim 5, wherein the first and second photodiodes included in the unit cells are arranged in the oblique direction to the row or column direction of the matrix arrangement (Col 4, Line 39 - 47).

9. Regarding claim 7, A CMOS image sensor according to Claim 6, wherein:

The unit cells are formed as an integrated circuit on a semiconductor substrate (Col 12, Line 55 – 58) and

The first and second photodiodes arranged in the oblique direction share the floating junction area, the reset drain area, the reset transistors, the driver transistors, the address transistors, the junction area between the driver transistors and the address

transistors and the diffusion area at the connecting portion between the driver transistors and the signal output line, thereby reading signals of the first pixel row and the second pixel row independently (See Figure 2 and Figure 21, Col 4, Line 39 – 47).

10. Regarding claim 8, A CMOS image sensor according to an embodiment of the present invention comprises:

A plurality of unit ceils (Figure 21, Element 81) arranged in the row and column directions at a predetermined pitch respectively in a two-dimensional plain forming a matrix, which include a first and a second photoelectric conversion element,

A first and a second transfer transistor (Figure 1, Element MTX3 and Element MTX2) for transferring charges stored by the photoelectric conversion elements at their common floating junctions (Col 13, Line 59 – 67 to Col 14, Line 1 – 65),

Reset transistors (Figure 1, Element MRES) for resetting the potential of the floating junctions,

Driver transistors (Figure 1, Element MSF) whose output potential is controlled by the potential of the floating junctions, and

Address transistors (Figure 22, Element 110) for selectively driving the driver transistors;

Reset drain voltage lines (Figure 22, Element 112) provided in the column direction of the matrix arrangement for resetting the potential of the common floating junctions included in the unit cell belonging to each column of the matrix arrangement (Col 13, Line 62 – 67);

First transfer lines (Figure 22, Element 108a) provided in the row direction of the matrix arrangement for controlling the first transfer transistor included in the unit cell belonging to each row (Col 13, Line 59 – 67 to Col 14, Line 1 – 65);

Second transfer lines (Figure 22, Element 108c) in the row direction of the matrix arrangement for controlling the second transfer transistors included in the unit cells belonging to each row of the matrix arrangement (Col 13, Line 59 – 67 to Col 14, Line 1 – 65);

First signal output lines (Figure 22, Element 107) provided in the column direction of the matrix arrangement to which the output voltages of the driver transistors included in the unit cells arranged in the odd numbered rows are supplied (Col 8, Line 60 – 67 to Col 9 Line 1 – 8);

Second signal output lines (Figure 22, Element 107) provided in the column direction of the matrix arrangement to which the output voltages of the driver transistors included in the unit cells arranged An the even numbered rows are supplied (Col 8, Line 60 – 67 to Col 9 Line 1 – 8); and

Address lines (Figure 22, Element 110) provided in the row direction of the matrix arrangement for selectively driving the driver transistors included in the unit cell belonging to each row (Col 13, Line 59 – 67 to Col 14, Line 1 – 65);

wherein image signals of the pixel arrays composed of the photoelectric conversion elements included in the unit cells arranged in the neighboring two columns are read simultaneously using the first and second signal output lines (Col 13, Line 59 – 67 to Col 14, Line 1 – 65).

11. Regarding claim 9, A CMOS image sensor according to Claim 8, wherein the adjacent pixel lines, which are read simultaneously, are a pixel row formed by the second photoelectric conversion elements included in the unit cell belonging to the first row and a pixel row formed by the first photoelectric conversion element included in the unit cell belonging to the second row, thereby simultaneously read the image signals of the pixel of adjacent tow rows into the first and second signal output lines by respectively supplying the same transfer pulse to the second transfer line provided for the unit cell belonging to the first row and the first transfer line provided for the unit cell belonging to the second row (See Figure 2, 21 – 22 and Col 13, Line 59 – 67 to Col 14, Line 1 – 65).

12. Regarding claim 10, A CMOS image sensor according to Claim 9,

A gate of the second transfer transistor included in the unit cell belong to the first row and a gate of the first transfer transistor included in the unit cell belong to the second row are connected to each other (See Figure 2, 21 – 22 Col 13, Line 59 – 67 to Col 14, Line 1 – 65).

13. Regarding claim 11, A CMOS image sensor according to Claim 10, wherein the first pixel row composed of the first photoelectric conversion element included in the unit cells belonging to the respective rows of the matrix arrangement and the second pixel row composed of the second photoelectric conversion element included in the unit cells

are independently read respectively by the first and second transfer lines (See Figure 2, 21 – 22 and Col 13, Line 59 – 67 to Col 14, Line 1 – 65).

14. Regarding claim 12, A CMOS image sensor accordin9 to Claim 11, wherein the first pixel row and the second pixel row are read by switching the first and second transfer transistors by the first and second transfer lines (See Figure 2, 21 – 22 and Col 13, Line 59 – 67 to Col 14, Line 1 – 65).

15. Regarding claim 13, A CMOS image sensor according to Claim 12, wherein the driver transistors and the address transistors, which are included in the unit cells are connected in series, wherein the first and second photoelectric conversion elements are connected no gate electrodes of the driver Transistors via the first and second transfer transistors, and wherein source electrodes of the reset transistors are connected to the gate electrodes of the driver transistors (See Figure 2, 21 – 22 and Col 13, Line 59 – 67 to Col 14, Line 1 – 65).

16. Regarding claim 14, A CMOS image sensor according to Claim 13, wherein the first and second photoelectric conversion elements are photodiode (Figure 21, Element 82a – 82d are photodiodes).

17. Regarding claim 15, A CMOS image sensor according to Claim 14, wherein the first and second photodiodes included in the respective unit cells are arranged in the

oblique direction to the row or column direction of the matrix arrangement (Col 4, Line 39 - 47).

18. Regarding claim 16, ACMOS image sensor according to Claim 15, wherein the unit cells are formed as an integrated circuit on a semiconductor substrate and wherein the first and second photodiodes arranged in the oblique direction share the floating junction area, the reset drain area, the reset transistors, the driver transistors, the address transistors, the junction area between the driver transistors and the address transistors, and the diffusion area at the connecting portion between the driver transistors and the signal output line, thereby reading signals of the first pixel row and the second pixel row independently (See Figure 2, 21 – 22 and Col 13, Line 59 – 67 to Col 14, Line 1 – 65).

19. Regarding claim 17, A CMOS image sensor according to Claim I, wherein among unit cells arranged in adjacent two rows of the matrix arrangement, a gate of the address transistor included in the unit cell arranged in the first row and a gate of the reset transistor included in the unit cell arranged in the second row are connected, and while an image signal from the second photoelectric conversion element included in the unit arranged in the first row is being read, the floating junction included in the unit cell arranged in the second row to be read next is reset, thus an image signal from the first photoelectric conversion element included in the unit cell arranged in the second row can be read (See Figure 2, 21 – 22 and Col 13, Line 59 – 67 to Col 14, Line 1 – 65).

20. Regarding claim 18, A CMOS image sensor according to Claim I7, wherein a first pixel row composed of the first photoelectric conversion element included in the unit cell belonging to each row of the matrix arrangement and a second pixel row composed of the second photoelectric conversion element included in the unit cell are independently read by the first and second transfer lines (See Figure 2, 21 – 22 and Col 13, Line 59 – 67 to Col 14, Line 1 – 65).

21. Regarding claim 19, A CMOS image sensor according to Claim 18, wherein the first pixel row and the second pixel row are read by switching the first and second transfer transistors by the first and second transfer lines (See Figure 2, 21 – 22 and Col 8, Line 60 – 67 to Col 9 Line 1 – 8, Col 13, Line 59 – 67 to Col 14, Line 1 – 65).

22. Regarding claim 20, A CMOS image sensor according to Claim 19, wherein the driver transistors and the address transistors which are included in the unit cells are connected in series, and the first and second photoelectric conversion elements are connected to gate electrodes of the driver transistors via the first and second transfer transistors, and source electrodes of the reset transistors are connected to the gate electrodes of the driver transistors (See Figure 2, 21 – 22 and Col 13, Line 59 – 67 to Col 14, Line 1 – 65).

23. Regarding claim 21, A CMOS image sensor according to Claim 19, wherein the first and second photoelectric conversion elements are photodiodes (Figure 21, Element 82a – 82d are photodiodes).

24. Regarding claim 22, A CMOS image sensor according to Claim 20, wherein the first and second photodiodes included in the unit cells are arranged in the oblique direction to the row or column direction on the matrix arrangement (Col 4, Line 39 - 47).

25. Regarding claim 23, A CMOS image sensor according to Clalm21, wherein unit cells are formed as an integrated circuit on a semiconductor substrate and the first and second photodiodes arranged in the oblique direction share the floating junction area, the reset drain area, the reset transistors, the driver transistors, the address transistors, the junction area between the driver transistors and the address transistors, and the diffusion area at the connecting portion between the driver transistors and the signal output line, thereby read signals of the first pixel row and the second pixel row independently (See Figure 2, 21 – 22 and Col 13, Line 59 – 67 to Col 14, Line 1 – 65).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SELAM T. GEBRIEL whose telephone number is (571)270-1652. The examiner can normally be reached on Monday-Thursday 7.30am-5.00pm.If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hai Tran can be reached on 571-272-7305. The fax phone

number for the organization where this application or proceeding is assigned is 571-273-8300.Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Selam Gebriel
Thursday, January 17, 2008

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